CLAIMS

1. A thin membrane stencil mask, comprising:

a substrate having a primary surface and a secondary surface opposite the primary surface;

a thin membrane layer overlying the primary surface of the substrate;

a stress control layer overlying the thin membrane layer;

one or more cavities in the substrate extending from the secondary surface to the thin membrane layer; and

a semiconductor device layer pattern having one or more openings in the stress control layer and the thin membrane layer, the one or more openings forming a stencil pattern in the thin membrane stencil mask.

2. The thin membrane stencil mask of claim 1 wherein the thin membrane layer has a thickness substantially in a range of 40-200 nanometers.

3. The thin membrane stencil mask of claim 1 wherein the stress control layer has a thickness substantially in a range of five to sixty nanometers.

4. The thin membrane stencil mask of claim 1 wherein a combined stress of the stress control layer and the thin membrane layer is in a range of 0 to 150 MPa.

5. The thin membrane stencil mask of claim 1 wherein a thickness of the stress control layer and the thin membrane layer in combination is between fifty and three hundred nanometers.

6. The thin membrane stencil mask of claim 1 wherein the stress control layer is controlled to have a predetermined stress factor by annealing the stress controlled layer during manufacture of the thin membrane stencil mask.

7. The thin membrane stencil mask of claim 1 wherein stress control can be achieved by a combination of compressive and tensile properties of the thin membrane layer and the stress control layer.

8. The thin membrane stencil mask of claim 1 wherein the thin membrane layer is comprised of silicon nitride.

9. The thin membrane stencil mask of claim 1 wherein the stress control layer is comprised of a metal or a metal alloy film.

10. The thin membrane stencil mask of claim 9 wherein the stress control layer is comprised of TaSiN, TaN, TaSiO, Cr or W.

11. The thin membrane stencil mask of claim 1 wherein the stress control layer is amorphous in microstructure.

12. The thin membrane stencil mask of claim 1 wherein at least one of the stress control layer and thin membrane layer exhibit contrast greater than 40% at an inspection radiated wavelength substantially in the range of 157 nanometers through 800 nanometers.

13. The thin membrane stencil mask of claim 1 further comprising:

a layer of carbon overlying the stress control layer and removed at the one or more openings, the layer of carbon absorbing radiation ions thereby enhancing material stability of materials previously deposited.

14. The thin membrane stencil mask of claim 13 wherein the layer of carbon has a thickness substantially in a range of 100-200 nanometers.

15. A method of forming a semiconductor device using a thin membrane stencil mask, comprising:

forming a resist on a semiconductor wafer having a plurality of semiconductor die;

projecting radiation through the thin membrane stencil mask and onto the resist formed on the plurality of semiconductor die, the radiation forming a contrast image on the resist, wherein the thin membrane stencil mask comprises:

a substrate having a primary surface and a secondary surface opposite the primary surface;

a thin membrane layer overlying the primary surface of the substrate;

a stress control layer overlying the thin membrane layer;

one or more cavities in the substrate extending from the secondary surface to the thin membrane layer;

a semiconductor device layer pattern having one or more openings in the stress control layer and the thin membrane layer, the one or more openings forming a stencil pattern in the thin membrane stencil mask; and

developing the resist.

16. The method of claim 15 further comprising:

depositing a layer of carbon overlying the stress control layer; and

etching the layer of carbon at corresponding one or more openings in the stress control layer, the layer of carbon absorbing radiation ions, thereby enhancing material stability of materials previously deposited.

17. The method of claim 15 wherein the thin membrane layer has a thickness substantially in a range of 40-200 nanometers.

18. The method of claim 15 wherein the stress control layer has a thickness substantially in a range of five to sixty nanometers.

19. The method of claim 15 wherein a combined stress of the stress control layer and the thin membrane layer is in a range of 0 to 150 MPa.

20. The method of claim 15 wherein a thickness of a combination of the stress control layer and the thin membrane layer is between fifty and three hundred nanometers.

21. The method of claim 15 wherein the stress control layer is controlled to have a predetermined stress factor by annealing the stress control layer during manufacture of the thin membrane stencil mask.

22. The method of claim 15 wherein stress control can be achieved by a combination of compressive and tensile properties of the thin membrane layer and the stress control layer.

23. The method of claim 15 wherein the thin membrane layer is comprised of silicon nitride.

24. The method of claim 15 wherein the stress control layer is comprised of a metal or a metal alloy film.

25. The method of claim 15 wherein the stress control layer is comprised of TaSiN, TaN, TaSiO, Cr or W.

26. The method of claim 15 wherein the stress control layer is amorphous in microstructure.

27. The method of claim 15 wherein at least one of the stress control layer and thin membrane layer exhibit contrast greater than 40% at an inspection radiated wavelength substantially in a range of 157 nanometers through 800 nanometers.

28. A method of fabricating a thin membrane stencil mask comprising:

providing a substrate having a primary surface and an opposite secondary surface;

forming an overlying thin membrane layer adjacent the primary surface;

forming an underlying hard mask layer adjacent the secondary surface;

forming a stress control layer overlying the thin membrane layer for adding strength to the thin membrane stencil mask, wherein the stress control layer is formed such that a desired combined stress of the stress control layer and the thin membrane layer is in a range of 0-150MPa;

etching one or more cavities through the hard mask layer and substrate and extending to the thin membrane layer;

defining a semiconductor device pattern in a resist layer overlying the stress controlled layer and the thin membrane layer, the semiconductor device pattern laterally overlying the one or more cavities; and

using the resist layer as a mask to etch the stress control layer and the thin membrane layer to form stencil holes for the purpose of permitting a radiation source to freely pass through the stencil holes.

29. The method of claim 28 wherein the thin membrane layer has a thickness substantially in a range of 40-200 nanometers.

30. The method of claim 28 wherein the stress control layer has a thickness substantially in a range of five to sixty nanometers.

31. The method of claim 28 wherein the stress control layer is annealed to achieve the desired combined stress.

32. The method of claim 28 wherein a full thickness of both the stress control layer and the thin membrane layer is between fifty and three hundred nanometers.

33. The method of claim 28 wherein the stress control layer is controlled to have a predetermined stress factor by annealing the stress control layer during manufacture of the thin membrane stencil mask.

34. The method of claim 28 wherein stress control can be achieved by a combination of compressive and tensile properties of the thin membrane layer and the stress control layer.

35. The method of claim 28 wherein the thin membrane layer is comprised of silicon nitride.

36. The method of claim 28 wherein the stress control layer is comprised of a metal or a metal alloy film.

37. The method of claim 28 wherein the stress control layer is comprised of TaSiN, TaN, TaSiO, Cr or W.

38. The method of claim 28 wherein the stress control layer is amorphous in microstructure.

39. The method of claim 28 wherein at least one of the stress control layer and thin membrane layer exhibit contrast greater than 40% at an inspection radiated wavelength substantially in a range of 157 nanometers through 800 nanometers.